REMARKS

Claim Rejections – 35 USC 102, 103

Regarding claims 1-21, Applicants respectfully disagree with the Examiner's arguments. Applicants respectfully point out that the blocks and signals illustrated in FIG. 3 of US Patent Application Publication 2004/0248624 (herein referred to as Leclercq) do not have the functions expressly required in the claims. For example, the Examiner argues that the signal ckvtcxo_in going into the clock generator 305 is a "power control mode indicator selecting a first power mode". Applicants respectfully point out that the Leclercq specification describes the ckvtcxo_in signal as one of the signals (along with ckvtcxo_out and vtcxo_en) which may be used to control a voltage/temperature controlled crystal oscillator (vtcxo) (see Leclercq, paragraphs 0034-0035). The ckvtcxo_in signal is the only input signal to the clock domain generator. The ckvtcxo_in signal must be the oscillating signal from the crystal oscillator. The ckvtcxo_in signal has nothing to do with "selecting a first power mode".

Next, the Examiner argues that the input provided from OR gate 340 of Leclercq is a trigger signal "triggering at least a first module to enter said first low power mode". But Leclercq teaches just the opposite. Leclercq teaches that wakeup signals are combined by OR gate 340 and provided to clock generator 305 as a wakeup signal (see Leclercq, paragraph 0037). The input provided by OR gate 340 of Leclercq is a wakeup signal, not a trigger signal to enter low power mode.

Next, the Examiner argues that the clr_deep_sleep signal of Leclercq is a first request signal "requesting said first module to enter said first low power mode". But Leclercq teaches just the opposite. Leclercq teaches that the signal clr_deep_sleep is a wakeup signal (see Leclercq, paragraph 0035). Again, the signal taught by Leclercq is a wakeup signal, not a request signal to enter low power mode.

Next, the Examiner argues that the signal from block 310 to AND gate 350 of Leclercq is a first response signal "indicating that said first module is ready to enter said first low power mode". But Leclercq teaches that the clock domain control blocks (e.g. 310) themselves put themselves in sleep mode (see Leclercq, paragraph 0036). Leclercq teaches that the signal from block 310 to AND gate 350 is a signal saying that block 310 has already put itself to sleep (see Leclercq, paragraph 0036). To analogize, the signal taught by Leclercq says "I've already put

myself to sleep". The first response signal of the claimed invention says "I'm ready for you to put me to sleep". In Leclercq, block 310 is already asleep. In the claimed invention, the module is not asleep.

The dependent claims are allowable for at least the reasons given above.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact Susan C. Hill if there are any issues regarding this communication or the current Application.

Respectfully submitted,

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